A PRACTICAL WIDEBAND GaAs PHASE DETECTOR *

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ABSTRACT

A GaAs monolithic phase detector operating over the frequency range of 1 MHz to 8 GHz, with a phase detection sensitivity factor of up to 1.6 has been developed at TRW. The detector circuit consists of a doubly balanced transconductance multiplier which has a total of 7 FETs and requires only one DC bias point. The detector chip measures 30 x 35 MILS and has a DC power consumption of 100 mW.

Introduction

Analog multipliers are widely used as essential building blocks of communication systems for instantaneous frequency and phase measurement, AM and FM detection, phase locked loops, and demodulators. As phase detectors, multipliers can be used to reduce the complexity of many communication systems, such as BPSK signal processing systems.

As a part of an FET based BPSK demodulator, we have developed a monolithic GaAs phase detector at TRW which can be operated over a wide frequency band and requires a dc input power of about 100 mW. A number of these phase detectors were fabricated and have been RF characterized. The circuit description and measurement results will be presented in the next section. This is followed by a brief description of GaAs processing and RF characterization.

Design

The schematic of the balanced phase detector is shown in Figure 1. Self biasing has been used such that only one dc bias point is required to bias all transistors in the circuit. A small resistor at the source of each FET provides the desired gate to source voltage for each FET. The potential at the lower end of this resistor is transferred to the transistor gate through a high resistive path which provides good RF isolation between gate and source.

Each FET at the top of the figure has a gate width of 40μ. The FETs in the middle each have a width of 80μ since they carry twice as much current as the upper FETs. Similarly, the FET at the bottom which carries four times the current of the 40μ FETs has a gate width of 160μ. In this manner and with appropriate selection of resistor values, the circuit has been designed such that the same DC voltage appears across each FET.

A photomicrograph of the phase detector chip is shown in Figure 2. With four 3 pF blocking capacitors included, the chip measures 30 x 35 MILS. Note that 80 percent of the area is taken by the blocking capacitors and bonding pads. The active area of the chip measures 8 x 12 MILS.

Figure 3 shows the DC voltage distribution within the phase detector circuit. For simplicity, the phase detector has been represented by the six FETs shown in Figure 3. Ideally, the voltages at nodes 1A, 2A and 3A should be identical to the voltages at the respective nodes 1B, 2B and 3B. Also, the applied voltage must divide equally among the FETs such that the voltage at node 1A would equal 1/2 of the voltage at node 2A and 1/3 of the voltage at node 3A. The actual measured node voltages shown in this figure indicates that the deviations from ideal voltage distribution is at most 50 mV.

Circuit Fabrication

The phase detector circuits were fabricated using a planar process featuring multiple selective ion implantation and double layer photoresist liftoff. Planar isolation better than 10 Ω/□ was achieved by selectively implanting silicon ions into the semi-insulating substrate to form the FET channel and bulk resistors. Heavy dose ion implantation was also used to improve the ohmic contacts. The dose and implant energy used for the FET channel and bulk resistors were 3 x $10^{12}cm^{-2}$ and 170 KeV. The ions were implanted through 900A plasma enhanced CVD nitride. The N+ implant of 2 x $10^{13}cm^{-2}$ at 130 KeV into the ohmic contact regions resulted in a sheet resistivity of 200 ohm/□ and an estimated surface impurity concentration of 3 x $10^{18}cm^{-3}$.

The process started with a thorough cleaning of the substrate followed by plasma nitride

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deposition. Ohmic contact regions and FET channels were sequentially implanted through the nitride as masked by appropriate photoresist patterns. The wafer was then annealed at 850°C for 30 minutes in N_2 ambient.

A double layer photoresist liftoff technique similar to the one described by C. Li and J. Richards,[1] was used to lift off all the metal patterns which includes the source and drain contacts, gate and second level metals. Ohmic contact metal, Au/Ge/Ni/Au was E-beam deposited, lifted off and alloyed in N_2 at 400°C for 30 seconds. The specific contact resistance was of the order of 10^{-6}ohm-cm^2. A Ti/Al/Ti metal system of 6000Å thick was used to form the Schottky contacts for FET gates and first level interconnections. The FET gate length is 1μm. After the gate formation, 4000Å thick silox was deposited to provide isolation between the first and second metal layers. Vias were chemically etched with shallow sloped sidewalls to improve step coverage. The second metal layer consisting of 500Å Ti and 30,000Å Al was E-beam deposited and lifted off with double layer photoresist liftoff technique. The line width was 10μm and the minimum spacing was 5μm.

RF Characterization

The phase detector circuit performs a multiplication function such that with $v_1 = V_1 \sin\omega_1 t$ applied to the LO port and $v_2 = V_2 \sin\omega_2 t$ applied to the RF port, the output signal would be

$$v_o = K v_1 v_2 = K[V_1 \sin\omega_1 t]\,[V_2 \sin\omega_2 t]$$

$$= K \frac{V_1 V_2}{2} [\cos(\omega_1-\omega_2)t - \cos(\omega_1+\omega_2)t]$$

$$= V_o [\cos(-) - \cos(+)]$$

$$V_o = \frac{V_1 V_2}{2} K$$

where K is a measure of phase detection sensitivity.

Variation of K factor as a function of frequency is plotted in Figure 4. As shown, the K factor remains fairly constant over a wide frequency range. In fact, the operating range of phase detector extends to and beyond 11 GHz. A phase detector, measured recently, had a K factor of 1.5 at 8 GHz and .57 at 11 GHz.

Figure 5 is a plot of the K factor as a function of input power at 2 GHz. From this figure, it is seen that K factor remains essentially constant as the input power is changed from -20 dBm to +10 dBm. With input power level of up to 8 dBm, the phase detector has an ideal detector characteristic. As the input power is increased beyond 8 dBm, the output becomes triangular. An output voltage as large as 3 volts has been observed.

References

1. C. Li and J. Richards, "A High Resolution Double Layer Photoresist Structure for Liftoff Technology," 1980 International Electron Device Meeting, Technical Digest, p. 412.

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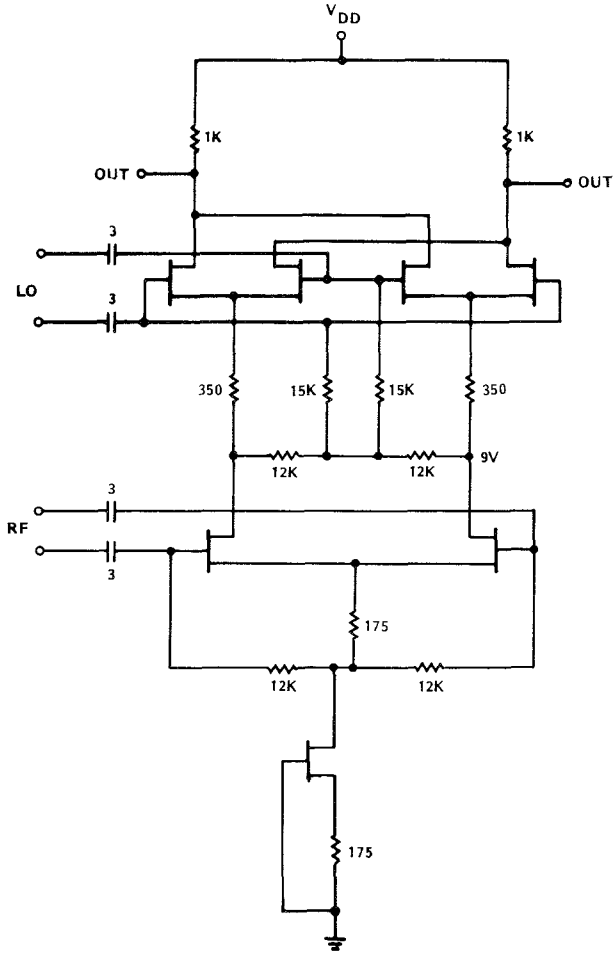

Figure 1. Circuit Schematic of the Phase Detector

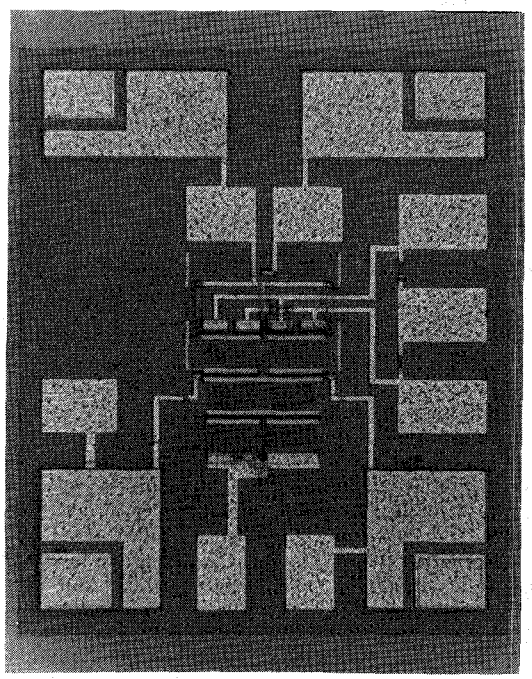

Figure 2. Photomicrograph of the Phase Detector

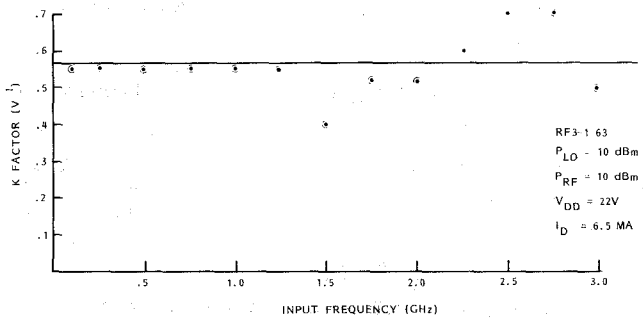

Figure 4. K Factor Vs. Input Frequency

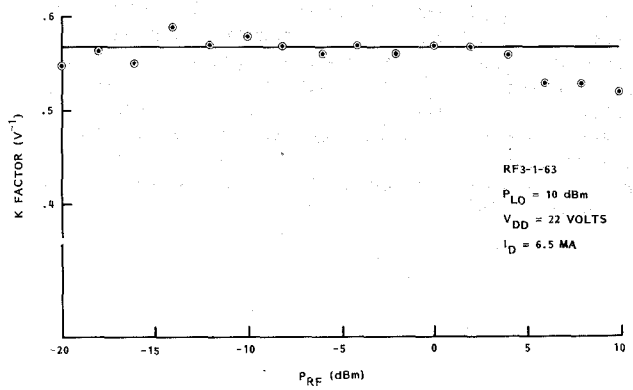

Figure 5. K Factor Vs. Input Power

VDD	8	10	12	13
V1A	1.04	1.15	1.20	1.22
V1B	1.04	1.15	1.20	1.22
V2A	2.10	2.32	2.41.	2.45
V2B	2.11	2.32	2.41	2.44
V3A	3.16	3.47	3.62	3.67
V3B	3.17	3.47	3.62	3.67

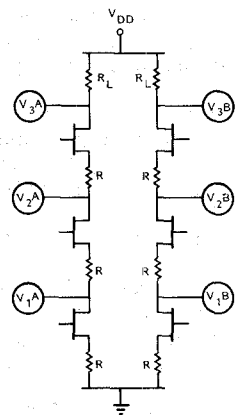

Figure 3. Phase Dectector DC Characterization RF3-12-2